CLAIMS

1. A system for testing an integrated circuit, the integrated circuit including flip-flops connected to a logic block and the test system including:

test means operable for connecting the flip-flops as a register, and

a plurality of types of inhibition means, each type of inhibition means being operable for inhibiting one specific type of element of the logic block capable of disturbing the sequencing of the register or the propagation of the signals into the logic block, and

control means for:

either operating the test means in synchronism with a command signal, or operating any one type of the plurality of types of inhibition means in synchronism with the command signal, or operating simultaneously the test means and any one type of the plurality of types of inhibition means in synchronism with the command signal ; and

operating continuously the other means.

2. The integrated circuit test system of claim 1, wherein elements of a first type condition the clock signal provided to at least one flip-flop.

3. The integrated circuit test system of claim 2, wherein said elements of the first type include means for activating or inactivating said clock signal.

4. The integrated circuit test system of claim 1, wherein elements of a second type condition a reset signal provided to at least one flip-flop.

5. The integrated circuit test system of any of claim 1, wherein elements of a third type include locking elements capable of preventing the propagation of at least one signal into the logic block.